AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A first hard-macro arranged on a semiconductor chip [[for]] and constituting a part of a semiconductor integrated circuit that includes plural blocks and plural hard-macros other than the first hard-macro that are connected to each other with signal wires, including at least one said signal wire passing through said first hard-macro ~~therethrough~~, wherein said at least one signal wire is formed in said first hard-macro before said first hard-macro is arranged on said semiconductor chip, and said at least one signal wire starts at a first outer edge of said first hard-macro and terminates at a second outer edge of said first hard-macro intersecting with said first outer edge.

2. (currently amended) The first hard-macro as set forth in claim 1, wherein said first and second outer edges are perpendicular to each other.

3. (currently amended) The first hard-macro as set forth in claim 1, wherein said first and second outer edges are adjacent to each other.

4. (currently amended) The first hard-macro as set forth in claim 1, wherein said at least one signal wire is L-shaped.

5. (currently amended) The first hard-macro as set forth in claim 1, wherein said at least one signal wire is linear.

6. (currently amended) ~~The hard-macro as set forth in claim 1~~ A hard-macro arranged on a semiconductor chip and constituting part of a semiconductor integrated circuit, said hard-wire macro comprising at least one wire passing therethrough that starts at a first outer edge of said hard-macro and terminates at a second outer edge of said hard-macro intersecting with said first outer edge,

wherein said hard-macro has a cut-out including ~~one of corners~~ a corner of said hard-macro, and said wire extends along said cut-out between said first and second outer edges.

7. (original) The hard-macro as set forth in claim 6, wherein said cut-out is rectangular, and said wire is L-shaped.

8. (currently amended) The first hard-macro as set forth in claim 1, further including a repeater inserted in said at least one signal wire.

9. (currently amended) The first hard-macro as set forth in claim 1, wherein said first hard-macro includes a plurality of said at least one signal wires passing therethrough.

10. (currently amended) The first hard-macro as set forth in claim 9, wherein said plurality of signal wires are equally spaced away from adjacent ones.

11. (currently amended) The first hard-macro as set forth in claim 9, wherein at least one of said plurality of signal wires includes a repeater inserted therein.

12. (currently amended) ~~The hard-macro as set forth in claim 1~~ A hard-macro arranged on a semiconductor chip and constituting part of a semiconductor integrated circuit, said hard-wire macro comprising at least one wire passing therethrough that starts at a first outer edge of said hard-macro and terminates at a second outer edge of said hard-macro intersecting with said first outer edge,

wherein said wire is divided into a plurality of portions each of which is arranged in each of a plurality of hierarchies of said hard-macro.

13. (currently amended) The first hard-macro as set forth in claim 1, wherein said first hard-macro is a random access memory (RAM).

14. (currently amended) The first hard-macro as set forth in claim 1, wherein said first hard-macro is a phase-locked loop (PLL) circuit.

15-16. (canceled)

17. (currently amended) A floor-planner ~~including a device for analyzing a floor-plan of a semiconductor integrated~~

~~circuit including a hard-macro arranged on a semiconductor chip for constituting a part of said semiconductor integrated circuit which hard-macro includes~~ comprising:

an input section, a controller, and a display section, said input section providing inputs to a program in said controller that causes said display section to display a floor-plan of a semiconductor device that includes a hard-macro;

the program analyzing the floor-plan and causing the floor-plan to include at least one wire passing ~~therethrough, wherein said wire is formed in said hard-macro before said hard-macro is arranged on said semiconductor chip, and said wire starts~~ through the hard-macro that extends from a first outer edge of said hard-macro and terminates at a second outer edge of said hard-macro intersecting with said first outer edge, wherein said wire is divided into a plurality of portions each of which is arranged in each of a plurality of hierarchies of said hard-macro.

18. (currently amended) The ~~floor-plan~~ floor-planner as set forth in claim 17, wherein ~~said device~~ the program analyzes a route of said wire.

19. (canceled)

20. (currently amended) The ~~program~~ floor-planner as set forth in claim [[19]] 23, wherein ~~said computer further~~ the program analyzes a route of said wire.

21. (new) The hard-macro as set forth in claim 6, wherein said hard-macro is a random access memory (RAM).

22. (new) The hard-macro as set forth in claim 6, wherein said hard-macro is a phase-locked loop (PLL) circuit.

23. (new) A floor-planner comprising:

an input section, a controller, and a display section, said input section providing inputs to a program in said controller that causes said display section to display a floor-plan of a semiconductor device that includes a hard-macro,

the program analyzing the floor-plan and causing the floor-plan to include at least one wire passing through the hard-macro that extends from a first outer edge of said hard-macro and terminates at a second outer edge of said hard-macro intersecting with said first outer edge,

wherein said hard-macro has a cut-out including a corner of said hard-macro, and said wire extends along said cut-out between said first and second outer edges.